In the Specification:

Page 1, after the title, insert the following paragraph:

--This is a divisional of Application Serial No. 09/570,026 filed May 12, 2000, the contents of which are incorporated herein by reference in their entirety.—

Please amend the following paragraphs to read as follows:

Paragraph beginning on page 2, line 15:

On the other hand, through recent ~~researches~~ research, the Inventors have come to realize that the use of the Ti_xO_y film as the adhesion layer between the ferroelectric capacitor and the SiO_2 film invites some undesirable problems, including deterioration of the ferroelectric property by diffusion of Ti into the PZT film, for example.

Paragraph beginning on page 2, line 26:

A feature of the invention is that, in semiconductor ~~device~~ devices having a ferroelectric capacitor which comprises a semiconductor substrate, and a ferroelectric capacitor composed of a lower electrode, ferroelectric film and upper electrode sequentially stacked on the semiconductor substrate via an insulating film, at least one of the upper and lower electrodes forming the ferroelectric capacitor is covered with a hydrogen barrier film which does not contain titanium.

Paragraph beginning on page 3, line 1:

In the present invention, the hydrogen barrier film not containing titanium is preferably a metal oxide film having a hydrogen diffusion constant of 10^{-5} cm^2/s or less. The hydrogen barrier film not containing titanium is required to have a high resistance if it is formed so as not to short-circuit the electrodes above on and under the ferroelectric capacitor. In this case, the metal oxide film preferably has a specific resistance not lower than 1 kΩcm. By making such a hydrogen barrier film on at least one of the base layer of the lower electrode and the upper surface of the upper electrode, deterioration in property of the ferroelectric film due to reduction by hydrogen is prevented. Additionally, by selecting an appropriate material for the hydrogen

barrier film, it functions as an adhesion layer and exfoliation of the capacitor formed on the insulating film is prevented.

Paragraph beginning on page 4, line 9:

In the present invention, the ferroelectric capacitor may be configured so that at least a part thereof from the lower electrode to the ferroelectric film ~~be~~ is buried in a groove formed in the insulating film. In this case, the hydrogen barrier film is buried in the groove so as to cover the bottom and side surfaces of the ferroelectric capacitor. The hydrogen barrier film may be brought into direct contact with the ferroelectric capacitor, or may be buried not to contact directly. In this case, the hydrogen barrier film is preferably formed also on the upper surface of the ferroelectric capacitor.

Paragraph beginning on page 5, line 17:

As the hydrogen barrier film interposed between the lower electrode of the ferroelectric capacitor and the insulating film, one having a small resistance is acceptable, and it is made of at least one kind of material selected from metal oxides such as Al_2O_3, Al_xO_y, $Al_xSi_yO_z$, AlN, WN, $SrRuO_y$, Ir_xO_y, Zr_xO_y, Ru_xO_y, Sr_xO_y, Re_xO_y, Os_xO_y, and Mg_xO_y. For the hydrogen barrier film, these metal oxides can be usable in either an amorphous state, a microcrystalline state, a polycrystalline state or a crystalline state. ~~It is the same also about~~ The same applies to the hydrogen barrier layer formed on the surface of the upper electrode of the ferroelectric capacitor.

Paragraph beginning on page 14, line 6:

The Al_2O_3 film 102 functions not only to ensure adhesion of the hard mask material film but also to protect the capacitor material film from damage in the process for stacking the ~~had~~ hard mask material film.

Paragraph beginning on page 16, line 6:

Figs. 6 through 11 are cross-sectional views showing a manufacturing process of a ferroelectric capacitor of ferroelectric random access memory according to the second embodiment of the invention. In this embodiment, a hydrogen barrier film is made merely on the upper surface of the upper electrode of the ferroelectric capacitor. First as shown in Fig. 6, after a transistor (not shown) is made on the silicon substrate 1, its surface is covered by an inter-layer

insulating film 2 of silicon oxide, for example, to level it. On the inter-layer insulating film 2, a lower Pt electrode film 30, approximately 100 nm thick, is stacked thereon by sputtering, for example, via an adhesion layer 201 not containing titanium. On the lower Pt electrode film 30, a PZT film 4, about 150 nm thick, is stacked by sputtering or sol-gel technique, for example. After that, the PZT film 4 is processed by RTA (rapid thermal annealing) in an oxygen atmosphere of 650°C, for example, to crystallize it.

Paragraph beginning on page 18, line 15:

On the upper Pt electrode film 50, a SiO_2 film 302 ~~if~~ is stacked by plasma CVD, and this SiO_2 film 302 is patterned as a hard mask. Then as shown in Fig. 13, the upper Pt electrode film 5 and the PZT film 4 are sequentially processed by etching. This etching is conducted until etching a part of the surface of the lower Pt electrode film 30.

Paragraph beginning on page 18, line 31:

After that, as shown in Fig. 15, a hard mask of SiO_2 film 304 covering the capacitor region is again patterned, and using this mask, the hydrogen barrier film 303, the lower Pt electrode film 3 and adhesion layer 301 are processed by etching to make up the ferroelectric capacitor C. Then, the mask is removed, and as shown in Fig. 16, an inter-layer insulating film 6 is stacked, a contact hole is made, and a terminal wiring 7 is formed.

Paragraph beginning on page 20, line 20:

Also in this embodiment, as the hydrogen barrier film 402, a metal oxide film having a hydrogen diffusion constant of 10^{-5} cm^2/s or less and preferably has a specific resistance not lower than 1 kΩcm is desirable, and representative one of such films is an Al_2O_3 film. By interposing the hydrogen barrier film inside the inter-layer insulating film in this manner, deterioration of the performance of the ferroelectric capacitor is prevented. The hydrogen banner film inside the inter-layer insulating film also functions to protect the ferroelectric capacitor from damage in a final process of stacking a passivation film (normally a SiN_x film) to cover the top surface of the device. Further, the inter-layer insulating film 6a functions to prevent interaction between the hydrogen barrier film and the ferroelectric capacitor C by direct contact thereof. Furthermore, the embodiment provided the effect of preventing diffusion of Pb ~~into~~ out of the

PZT film, and the effect of preventing diffusion of Ti into the PZT film because Ti is not used. Additionally, since the Al_2O_3 film is an insulating film, it can be inserted in the entire area of the inter-insulating film without patterning, and short-circuiting of a contact to the diffusion layer does not occur.

Paragraph beginning on page 21, line 27:

If the hydrogen barrier film 402 (Al_20_3, Al_xO_y, $Al_xSi_yO_z$, Ti_xO_y, etc.) is stacked directly ~~of~~ on the capacitor, oxygen contained in the ferroelectric film 4 is trapped by the hydrogen barrier film 402, and deterioration of the property is liable to occur. Such deterioration of the property is recovered for a while by oxygen annealing. However, when the process progresses to a step not including oxygen annealing, if a reducing gas such as hydrogen again reaches the hydrogen barrier film 402, a certain portion in the hydrogen barrier film is reduced, and the reduced element (Al, Ti) traps oxygen of the ferroelectric film 4 and deteriorates its property.

Paragraph beginning on page 22, line 19:

The method for making the first insulating film 6a is desired to satisfy the requirements: (1) the atmosphere is unlikely to generate hydrogen radicals or does not generate much; (2) the temperature is low (preferably not higher than 400°C); (3) the stacked film is not too thick beyond a required thickness (because deterioration by hydrogen radicals will occur during deposition and because the ~~pattering~~ patterning and/or opening of the film become more difficult as the thickness becomes greater); and (4) taking its coverage into consideration, its thickness is thicker than 0.05 times and smaller than three times of the thickness of the capacitor (sum of the upper electrode 5, ferroelectric film 4 and lower electrode 3 (including a barrier metal)).

Paragraph beginning on page 32, line 28:

In the dry etching step of the PZT film 4, lower Pt electrode film 3 and hydrogen barrier film 801, there is used an etching condition which ensure that side surfaces of the PZT film 4 and the lower Pt electrode film 30 become near to vertical surfaces, more specifically, sharp slopes having an angle not lower than ~~75°C~~ 75°. When this etching condition is used, a re-deposit film 804 is formed on side surfaces of the PZT film 4 and the lower Pt electrode 3 after processed as shown in Fig. 42. Although this re-deposit film 804 contains etched substances from the

hydrogen barrier film 801, and from the PZT film 4, Pt films, SiO_2 films, etc., since it contains the substance of the hydrogen barrier film, it exhibits a certain hydrogen barrier effect.

Paragraph beginning on page 35, line 2:

Regarding the leak characteristics, when the leak current responsive to application of d.c. 5V exceeds 10^{-4} A/cm^2, it was evaluated as being bad "B". For total evaluation, ~~horny~~ ratios of spontaneous polarization characteristics were taken into consideration in addition to leak characteristics.

Paragraph beginning on page 35, line 25:

Fig. 46 shows the spontaneous polarization amount (solid line) of the test sample No. 4 after a fatigue test (a stress of a.c. 5V is applied with the pulse width of 20 μS is applied 3^{10} times) together with the initial state (broken line). Fig. 47 shows a relation between the number of fatigue tests and the spontaneous polarization amount. It is known from Fig. 46 that, as compared with the initial state of about 20 μC/cm^2, the value becomes 30 μC/cm^2 after fatigue, and the property is improved ~~than~~ compared to the initial status.

Paragraphs beginning on page 39, line 28:

After these films are made, a ~~had~~ hard mask material 33 of silicon oxide or silicon nitride, for example, is ~~tacked~~ stacked, and a resist pattern 35 is formed and patterned thereon (Fig. 58). Then, a hard mask material 33 is patterned by anisotropic etching, and the resist pattern is removed by ashing. Thereafter, the upper electrode material film 50 is etched to pattern the upper electrode 5 (Fig. 59).

After that, a ~~had~~ hard mask material 34 is again stacked (Fig. 60). The ~~had~~ hard mask material 34 is preferably the same material as the hard mask material 33 used before, but a different material is also acceptable therefor. The hard mask material 34 has a thickness in the range from substantially the same as the thickness of the PZT film 4 to less than twice the same. Its reason is that, because the electric line of force passing from an end of the upper electrode 5 to the lower electrode extends to outside by about the thickness of the PZT film 4, an equivalent side wall thickness is required. Further, taking alleviation of process damage into consideration,

it is preferable that the side walls are amply thick, but from the viewpoint of miniaturization, this degree of film thickness is the optimum thickness.